PATENT CLAIMS

1. Circuit arrangement for bridging high voltages using a switching signal, characterized in that,

a voltage transmitter (2) with first and second terminals (7/Vdd, 8Vss) for a low voltage and a voltage receiver (1) with third and fourth terminals (11/Vddh1/ 12/Vddh2) for a higher voltage relative to the small voltage between the first and second terminals (7/Vdd, 8/Vss) each comprise a first inverter circuit and a second inverter circuit, wherein the inverter circuits of the voltage transmitter (2) are connected between the first and second terminals (7/Vdd, 8/Vss) and the inverter circuits of the voltage receiver (1) are connected between the third and fourth terminals (11/Vddh1, 12/Vddh2), in that the outlet of the first inverter circuit (3) of the voltage transmitter (2) is connected via a first capacitor (C1) as high voltage capacitor with the inlet of the second inverter circuit (4) of the voltage receiver (1) and the outlet of the first inverter circuit (5) of the voltage receiver (1) and inthat the outlet of the second inverter circuit (4) of the voltage transmitter (2) is connected via a second capacitor (C2) as a high voltage capacitor with the inlet of the first inverter circuit (5) of the voltage receiver (1) and the outlet of the second inverter circuit (5) of the voltage receiver (1), in that the inlets of the first inverter circuit (3) and the second inverter circuit (4), respectively, of the voltage transmitter (2) are a non-inverted and an inverted inlet and that the outlets of the first inverter circuit (5) and the

second inverter circuit (6), respectively, of the voltage receiver (1) represent outlet nodes.

2. Circuit arrangement of claim 1, characterized in that,

a third inverter circuit (15) is connected between the first and second terminals (7/Vdd, 8/Vss), in that the outlet of the third inverter circuit (15) is connected with the inlet of the first inverter circuit (3) of the voltage transmitter (2), in that the inlet of the third inverter circuit (15) is connected with the inlet of the second inverter circuit (4) of the voltage transmitter (2), and in that the inlet of the third inverter circuit (15) is connected with the terminal IN (16) as the inlet of the circuit assembly for bridging high voltages with a switching signal.

3. Circuit arrangement of claim 1, characterized in that,

a fourth inverter circuit (17) and a fifth inverter circuit (18) are connected between the third and fourth terminals (11/Vddh1, 12/Vddh2), in that the inlet of the fourth inverter circuit (17) is connected with the inlet of the first inverter circuit (5) of the voltage receiver (1), in that the inlet of the fifth inverter circuit (18) is connected with the inlet of the second inverter circuit (6) of the voltage receiver (1), in that the outlet of the fourth inverter circuit (17) is connected with the terminal OUT1 (19) as the first outlet of the voltage receiver (1), and in that the outlet of the fifth inverter circuit (18) is connected with the terminal OUT2 (20) as the second outlet of the voltage receiver (1).

4. Circuit arrangement of claim 1 through 3, characterized in that

a sixth inverter circuit (21) and a seventh inverter circuit (22) are connected between the first and second terminals (7/Vdd, 8/Vss), in that the inlet of the seventh inverter circuit (22) is connected with the inlet of the third inverter circuit (15) and with the terminal IN (16) as the inlet of the circuit arrangement for bridging high voltages with a switching signal, in that the outlet of the seventh inverter circuit (22) is connected with the inlet of the sixth inverter circuit (11) and in that the outlet of the sixth inverter circuit (21) is connected with the inlet of the second inverter circuit (4) of the voltage transmitter (2).

5. Circuit arrangement of claims 1 through 4, characterized in that

an inverter circuit comprises two complementary transistors connected in series.

6. Circuit arrangement of claim 1, characterized in that

the first capacitor (C) and the second capacitor (C2) are connected between the voltage transmitter (2) and the voltage receiver (1) in such a way that the first capacitor (C1) and the second capacitor (C2), respectively, are charged as high voltage capacitors to the voltage differential to be overcome between the voltage transmitter (2) and the voltage receiver (1) and their charge subsequently varies at the value $\Delta Q = C \times (Vdd - Vss)$ for signal transmission, whereby the

power consumption of the circuit arrangement for bridging high voltages with a switching signal is independent from the voltage differential to be overcome between the voltage transmitter (2) and the voltage receiver (1) and simultaneously, the applied differential principle (C1 is charged at ΔQ, C2 is discharged at ΔQ, and vice versa) guarantees a high signal to noise ratio relative to push-push interference signals.

7. Circuit arrangement of claim 1, characterized in that,

the circuit arrangement for bridging high voltage with a switching signal is realized as an integrated semi-conductor circuit made with semi-conductor processes on the one hand with CMOS circuits as the inverter circuits and, on the other hand, a stack of layers with circuit stopper implantation, field oxide, poly-silicon, CVD-oxide, metal, CVD-oxide, metal, and so on, whereby the layers are electrically alternatingly connected, as the first capacitor (C1) and as the second capacitor (C2), respectively, as high voltage capacitors.

8. Circuit arrangement of claims 1 through 7, characterized in that,

the voltage transmitter (2) is one region or multiple regions (23a, 23b) of the semi-conductor chip, in that the first capacitor (C1) is one region (24) and the second capacitor (C2) is one region (25) of the semi-conductor chip, and in that the voltage receiver (1) is one region (26) of the semi-conductor chip, and in that at least the region of the

voltage transmitter (2) and of the voltage receiver (1), respectively, are surrounded by trenches (27) for voltage isolation.

9. Circuit arrangement of claims 1 through 8, characterized in that,

the circuit arrangement for bridging high voltages with a switching signal is realized as integrated semi-conductor circuits made with semi-conductor processes for integrated high voltage circuits with any isolation for the voltage transmitter (2), the high voltage capacitors, and the voltage receiver (1).